A C-BAND 10 WATT GAAS POWER FET

J. Fukaya, M. Ishii, M. Matsumoto, Y. Hirano

Fujitsu Limited, Discrete Semiconductor Division
Kawasaki, Japan

Abstract

A new GaAs high power FET has been developed. The FET chip with 10.8mm gate-width employs a deep recess, via hole PHS, an air bridge gate-source cross-over and novel gate feeder network technology. The internally matched device which consists of two chips (total gate-width; 21.6mm) has realized 10 watts of 1dB gain compression power with 8dB gain and 43% power added efficiency at 8GHz.

Chip Design for High Efficiency

The key to high efficiency performance is as follows:

1) High drain to source breakdown voltage (BVds)
2) Low source resistance (Rs)
3) High gain

In order to achieve high BVds and low Rs, a deep recess structure is employed. For gain improvement, it is important to reduce all parasitic elements such as Cgb, Cgd, Ls, etc. An air bridge gate-source cross-over makes it possible to decrease the parasitic Cgs and the dielectric dissipation through the gate bus. A via-hole PHS technique is essential for reducing Ls and thermal resistance. For larger gate width devices, the phase difference between each gate finger degrades power combining, which decreases both gain and output power. A newly developed tree type gate feeder network provides an in-phase divided input signal to each gate finger. To realize the target performance, device parameters such as Cgs, Cgd and gm have been optimized by means of CAD.
The total gate width has been optimally determined to be 10.8mm in order to satisfy output power requirements and a unit gate width of 75μm.

Fig. 1 Photograph of 10.8mm Chip

Wafer Processing

As with conventional FET's, after mesa-isolation of the active area AuGe/Au source and drain electrodes are formed on an epitaxially grown n-GaAs wafer (N_D=1.5x $10^{17}/cm^3$) prior to making the channel recess. A one-micron-length Aluminum Schottky gate electrode is fabricated in the deeply recessed channel using the self-aligned method. The chip surface is passivated with silicon nitride. In the via-hole PHS process the GaAs wafer is thinned (t=25um), then through-holes for source grounding are formed. Plated gold forms the heat-sink and connects the surface source electrodes to the heat-sink. The total chip thickness is controlled to 60μm.

Internal Matching Network and Package

Internal matching for large gate width FET's is necessary because the input/output impedances are very low. CAD for the internal matching network has been done using a large signal equivalent circuit model, but only the drain conductance is considered to be a non-linear element. The input matching circuit consists of bonding wire inductance and capacitance made from a high dielectric constant material. The distributed output matching circuit is patterned on a Al_2O_3 substrate.

Also, a new resonance-free package has been developed. The package has a grounded metal side-wall and rectangular coaxial type input/output which improves the isolation characteristics, and ensures stable operation.

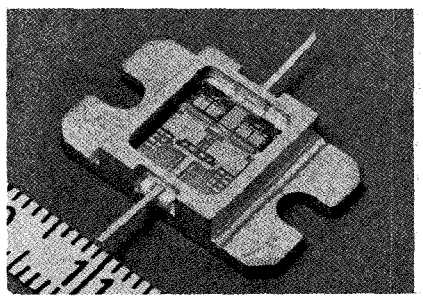

Fig. 2 Internally Matched Device

0149-645X/84/0000-0187 $01.00 © 1984 IEEE

RF Performance

Table 1 shows the DC characteristics of the internally matched one-chip and two-chip devices. Due to the via-hole PHS, the thermal resistance was reduced to 5.8°C/W and 3.1°C/W, respectively.

The Pin-Pout performance for the two-chip device is shown in Fig. 3. The measurement was done with a 50 ohm test fixture and input/output stub tuners for additional adjustment. The FET was biased at 10V through the bias circuits in the test fixture. The device showed 10W P1dB and 8dB G1dB at 8GHz with 40% power added efficiency. With 8.5V operation, a power-added efficiency of 43% was obtained at 39dBm Pout and 7dB gain.

Fig. 4 shows S_{11} and S_{22} of the two-chip device.

A two tone test was performed for the two-chip device. The measured third-order intermodulation distortion (IM_3) is shown in Fig. 5. At 33dBm output power, IM_3 was 41dBc. This value is more than 10dB lower than that for conventional TWT's.

Table 1 DC characteristics

	I_{dss} (A)	gm (mho)	Vp (V)	V_{gso} (V)	R_{th} (°C/W)
ONE-CHIP	1.95	0.9	-2.25	-14.0	5.8
TWO-CHIP	3.83	1.85	-2.03	-14.5	3.1

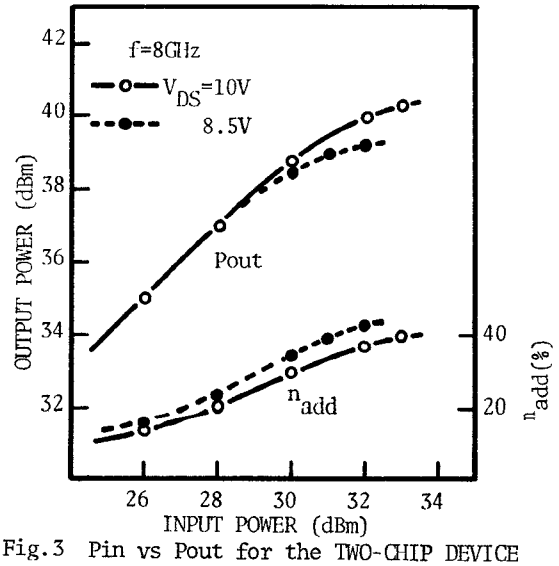

Fig.3 Pin vs Pout for the TWO-CHIP DEVICE

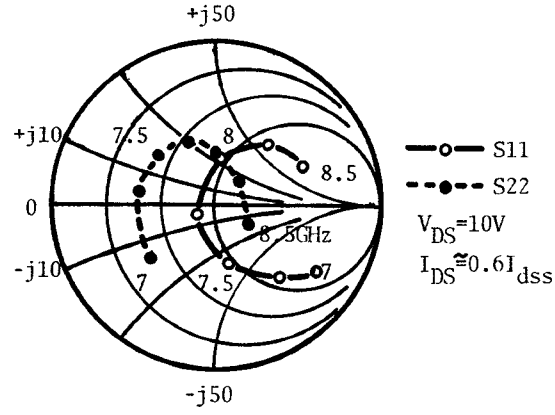

Fig.4 S11,S22 of the TWO-CHIP DEVICE

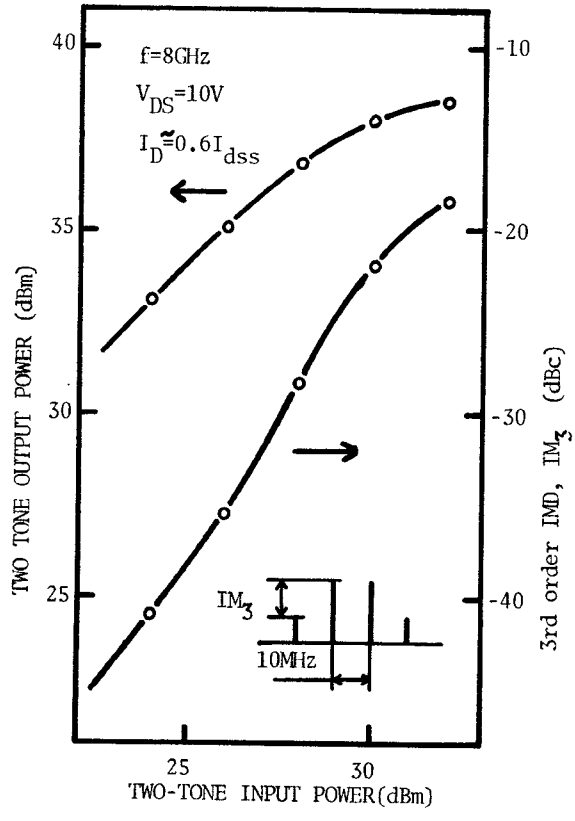

Fig. 5 IMD of the TWO-CHIP DEVICE

References

(1) Y. Hirachi, Y. Takeuchi, T. Matsumura, K. Ohta, K. Kosemura, and S. Yamamoto, "A Novel Via Hole P.H.S. structure in K-band power GaAs FET," in Int. Electron Devices Meeting Tech. Dig., pp. 676-679, Dec. 1981